REMARKS

Claims 1-9 and 34-41 are all the claims pending in the application. Claims 10-33 are canceled, above, pursuant to previously-filed Restriction Requirement. Claims 34-42 are added to further define the invention. Claims 3, 4, and 7 stand objected to only as being dependent upon a rejected base claim, and would be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims. Claims 2 and 7 have been rewritten in independent form to place them in condition for immediate allowance. Further, claims 1 and 6 have been rewritten in view of the prior art to broaden these claims, by removing limitations.

Claim 8 stands rejected upon informalities. Claims 1, 2, 5, 6, and 9 stand rejected on prior art grounds. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The 35 U.S.C. §112, Second Paragraph, Rejection

Claim 8 stands rejected under 35 U.S.C. §112, second paragraph. The dependency of claim 8 has been modified to eliminate the antecedent basis issues. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. The Prior Art Rejections

Claims 1, 2, 5, 6, and 9 stand rejected under 35 U.S.C. §102(e) as being anticipated by Lin et al., hereinafter "Lin" (6,762,448). Applicants respectfully traverse this rejection because Lin does not teach or suggest separate transistors that utilize closely spaced, yet insulated fins. Instead, Lin discloses a multi-fin transistor. As explained in greater detail below, the claimed invention defines a structure that includes multiple separate transistors, while Lin discloses a

single transistor that utilizes multiple fins.

One distinction between the claimed invention and the structure disclosed in Lin can be seen by comparing Figure 9 of Lin with Applicant's Figure 1. In Figure 9 of Lin, the transistor includes a single source contact 910 and a single drain contact 920 with multiple fins 810 connecting the source contact to the drain contact. To the contrary, as shown in Applicants' Figure 1, each separate transistor includes distinct source and drain contacts 108 that are separate from one another. Thus, the invention actually presents two very closely spaced, yet separate, transistors, each of which includes distinct source and drain contacts 108 and a separate fin 100, 102 separated by a fin insulator 104.

The claimed invention allows two or more FinFETs to be formed in the space where previously only one FinFET could be formed, thereby approximately doubling (quadrupling, etc.) the density of the FinFETs. The structure utilized by the invention is shown in Figure 1 which shows a top view. Figure 1 illustrates four fins 100, 102 that define four separate transistors. More specifically, the fins 100 form P-type field effect transistors (PFETs) and the fins 102 form N-type field effect transistors (NFETs). An insulator 104 separates the two fins. The gates which surround the channel regions of the fins are shown as items 106. The gate contacts are shown as items 112, while the contacts for the source and drain of the various transistors shown are labeled item 108. Item 110 represents an insulator region that can comprise the isolation region that separates the various transistors. While Figure 1 illustrates complementary N-type and P-type transistors, one ordinarily skilled in the art would understand that the structure is not limited to complementary type transistors and could comprise any form of transistor based structure. While the description focuses on an exemplar two-FinFET structure, one ordinarily skilled in the art would understand that the structure is not limited to pairs and multiple FinFETs could be formed.

As described above, the inventive process produces a structure that almost doubles the density of FinFET devices. The invention utilizes spacer technology to form the fins, which allows the fins of different transistors to be formed much closer together (only separated by one spacer width) and allows the fins to be sub-lithographic in size. The invention also provides for angled ion implants, which allows one fin to shield the other fin (in each set of fins) to permit the

fins to be selectively doped differently. Therefore, the invention easily produces complementary transistors. The complementary transistors share a gate and can be contacted individually allowing the formation of integrated circuits in a smaller area. The invention also provides a method to form pairs of fins that could be formed into transistors, or used as wires or resistors to contact each fin independently.

More specifically, the claims provide "an insulator fin positioned between said first fin and said second fin, and that "said first FinFET comprises a separate transistor from said second FinFET" (independent claims 1 and 6). Therefore, it is Applicants position that the claimed invention defines two separate transistors (which can be complementary transistors) that are separated by an insulator fin. This is different than the structure disclosed in Lin, because Lin describes a single transistor that includes multiple fins 810 separated by an insulating fin 210. With the claimed invention, because the transistors are separate from one another, they can be operated independently. To the contrary, because Lin describes a single transistor with single source and gate contacts, the separate fins cannot be operated as two separate transistors. That is, is Applicants position that Lin does not teach or suggest the claimed invention.

Thus, as shown above, Lin does not teach or suggest "an insulator fin positioned between said first fin and said second fin, and that "said first FinFET comprises a separate transistor from said second FinFET" (independent claims 1 and 6) and independent claims 1 and 6 are patentable over Lin. Further, dependent claims 2, 5, and 9 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-9 and 34-42, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 11/12/04

Frederick W. Gibb, III
Registration No. 37,629

McGinn & Gibb, PLLC
2568-A Riva Road
Suite 304
Annapolis, MD 21401
(410) 573-1545
Customer Number: 29154